REMARKS

Claims 1-7, 9 and 13 remain for further consideration. No new matter has been added.

The Applicant notes that Box 2 on PTOL-326 is checked non-final, which is appropriate considering the fact that with the last response an RCE was filed.

The objections and rejections shall be taken up in the order presented in the Official Action.

5-6. Claims 4 and 7 currently stand rejected under 35 U.S.C. §112, first paragraph as allegedly failing to comply with the enable requirement.

It is respectfully submitted that the specification clearly discusses the claim features in question in paragraphs [0025], [0026], [0045] and [0057], amongst others. In addition, the figures of the application clearly illustrate in detail several examples how the trellis decoder and filter taps are connected according to aspects of the invention. For example, paragraphs [0039] and [0053] of the specification discuss the structure of FIG. 11 comprising 12 parallel trellis decoders and 16 decoding stages). Such illustrations certainly provide the skilled person in this technical field with the information necessary to make and use the claimed invention without unnecessary experimentation.

7-8. Claims 1-7, 9 and 13 currently stand rejected for allegedly being obvious in view of published U.S. application 2002/0172275 to Birru (hereinafter "Birru") in view of Applicant's Admitted Prior Art (AAPA).

Claim 1 recites an adaptive equalizer comprising a Viterbi decoder having 16 stages and a decision feedback equalizer that has more than 16 taps. Assuming for the moment, without admitting that Birru and AAPA are even properly combinable, it is respectfully submitted that the resultant combination is still incapable of rendering claim 1 obvious since the resultant combination

fails to suggest the relationship that the number of decision equalizer taps is greater than the Viterbi decoder states. Specifically, Birru discloses that the number of trellis decoder stages is equal to the number of decision feedback equalizer taps. Birru states *"[t]he filter coefficients of decision feedback equalizer filter (DFEl) 720 at time k are* $g^k=\{g^k_1, g^k_2, \ldots, g^k_{N2}\}$*."* [¶0095] Thus, Birru clearly teaches that the decision feedback equalizer includes N2 taps. Similarly, Birru clearly states that the trellis decoder disclosed therein includes N2 stages with the statement *"[t]he outputs of trellis decoder 250 at time k are* $a^k=\{a^k_1, a^k_2, \ldots, a^k_{N2}\}$*."* [¶0096]. Also see ¶0096 and ¶0097 that disclose the DFE has N2 number of taps and the trellis decoder has N2 stages. There is simply no suggestion in Birru, or in the combination of Birru and the AAPA, that the number of taps in the decision feedback equalizer is greater than the number of stages in the trellis decoder.

The Official Action recognizes that *"Birru does not specify the Viterbi decoder having 16 stages and the decision feedback equalizer having more than 16 taps and a mapper element between the decoder and the decision feedback equalizer."* (Official Action, pg. 4). The Official Action then alleges *"[t]he AAPA further discloses the input into the decision feedback equalizer is the output of the mapper (Specification, Page 6, lines 15-16). The AAPA further discloses the decision feedback to include "M" stages (Specification, page 6, lines 16-20). Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention that the AAPA teaches implementing a Viterbi decoder comprising 16 stages ...in an 8VSB system."* (Official Action, pg. 5). However, as discussed in the background section of the present application, see paragraphs [¶0021] and [¶0022], the prior art shown in FIGs. 3 and 7 of the present application merely illustrate systems that employ structures were the decision feedback equalizer (DFE) is arranged before the trellis decoder, and therefore the DFE undesirable uses uncoded data. This is clearly discussed as a problem in the background section of the present application. In such prior art systems the DFE is running

independently from the trellis decoder (see paragraph [¶0022] of the present application). Accordingly, a skilled person would not look to the AAPA and its independent arrangement of the DFE and trellis decoder because of the undesirable results cited by the AAPA. The independent relationship of the DFE and trellis decoder roundly identified as a problem in the AAPA art would not provide any teaching to a skilled person regarding the particular claimed structure of the number of decoder stages (e.g., 16 in claim 1) versus the number of decision feedback equalizer taps (e.g., more than 16 taps in claim 1). A skilled person would not use the teachings of the AAPA to modify Birru because it would NOT result in a predictable system, since the system of Birru uses decoded data for the DFE, while the AAPA uses coded data as input to the DFE. Therefore, applying a teaching of the AAPA that uses a DFE operating with coded data, to a system such as Birru that employs a DFE operating on decoded data provides no predictable modification or reasonable motivation to combine.

Further, the express teachings of the AAPA states how undesirable it is to use a system that utilizes a DFE operating on coded data. Therefore, a skilled person would not see any predictable modification to Birru based upon the criticized approach discussed in the AAPA.

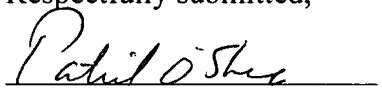
Thus, it is respectfully submitted that a fair and proper reading of Birru reveals that the combined teachings of Birru and AAPA are incapable of rendering claim 1 obvious.

Claims 4, 7 and 13 also recite the feature that the number of stages in the decoder is different than the number of taps in the decision feedback equalizer. Accordingly, it is respectfully submitted that these claims are patentable for at least the reasons set forth above.

Reconsideration and allowance of claims 1-7, 9 and 13 is respectfully requested. No new matter has been added.

If a telephone interview could assist in the prosecution of this application, please call the undersigned attorney.

Respectfully submitted,



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